What is claimed is:

1. A method of forming a gate oxide on a transistor body region, comprising:
evaporation depositing a metal alloy layer on the body region; and
oxidizing the metal alloy layer to form a metal oxide layer on the body region.

2. The method of claim 1, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

3. The method of claim 1, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

4. The method of claim 3, wherein electron beam evaporation depositing the metal alloy layer includes electron beam evaporation of a single metal alloy target.

5. The method of claim 1, wherein evaporation depositing the metal alloy layer includes evaporation depositing at an approximate substrate temperature range of 100 - 150° C.

6. The method of claim 1, wherein oxidizing the metal alloy layer includes oxidizing at a temperature of approximately 400° C.

7. The method of claim 1, wherein oxidizing the metal alloy layer includes oxidizing with atomic oxygen.

8. The method of claim 1, wherein oxidizing the metal alloy layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

9. A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal alloy layer on the body region; and

oxidizing the metal alloy layer using a krypton(Kr)/oxygen (O_2) mixed plasma process to form a metal oxide layer on the body region.

10. The method of claim 9, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

11. The method of claim 9, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

12. The method of claim 11, wherein electron beam evaporation depositing the metal alloy layer includes electron beam evaporation of a single metal alloy target.

13. The method of claim 9, wherein evaporation depositing the metal alloy layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

14. A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal alloy layer on the body region;

oxidizing the metal alloy layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

15. The method of claim 14, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

16. The method of claim 14, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

17. The method of claim 16, wherein electron beam evaporation depositing the metal alloy layer includes electron beam evaporation of a single metal alloy target.

18. The method of claim 14, wherein evaporation depositing the metal alloy layer includes evaporation depositing at an approximate substrate temperature range of 100 - 150° C.

19. The method of claim 14, wherein oxidizing the metal alloy layer includes oxidizing at a temperature of approximately 400 °C.

20. The method of claim 14, wherein oxidizing the metal alloy layer includes oxidizing with atomic oxygen.

21. The method of claim 14, wherein oxidizing the metal alloy layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

22. A method of forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal alloy layer on the body region;

oxidizing the metal alloy layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. The method of claim 22, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

24. The method of claim 22, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

25. The method of claim 24, wherein electron beam evaporation depositing the metal alloy layer includes electron beam evaporation of a single metal alloy target.

26. The method of claim 22, wherein evaporation depositing the metal alloy layer includes evaporation depositing at an approximate substrate temperature range of 100 - 150° C.

27. The method of claim 22, wherein oxidizing the metal alloy layer includes oxidizing at a temperature of approximately 400 °C.

28. The method of claim 22, wherein oxidizing the metal alloy layer includes oxidizing with atomic oxygen.

29. The method of claim 22, wherein oxidizing the metal alloy includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

30. A method of forming an information handling system, comprising:

forming a processor;

forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal alloy layer on the body region;

oxidizing the metal alloy layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

31. The method of claim 30, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

32. The method of claim 30, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

33. The method of claim 32, wherein electron beam evaporation depositing the metal alloy layer includes electron beam evaporation of a single metal alloy target.

34. The method of claim 30, wherein evaporation depositing the metal alloy layer includes evaporation depositing at an approximate substrate temperature range of 100 - 150 °C.

35. The method of claim 30, wherein oxidizing the metal alloy layer includes oxidizing at a temperature of approximately 400 °C.

36. The method of claim 30, wherein oxidizing the metal alloy layer includes oxidizing with atomic oxygen.

37. The method of claim 30, wherein oxidizing the metal alloy layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

38. A transistor, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a cobalt-titanium alloy oxide dielectric layer coupled to the surface portion of the body region; and

a gate coupled to the cobalt-titanium alloy oxide dielectric layer.

39. The transistor of claim 38, wherein the cobalt-titanium alloy oxide dielectric layer includes $CoTiO_3$.

40. The transistor of claim 38, wherein the surface portion of the body region is oriented in the (100) crystalline plane.

41. The transistor of claim 38, wherein the surface portion of the body region is oriented in the (111) crystalline plane.

42. The transistor of claim 38, wherein the cobalt-titanium alloy oxide dielectric layer is substantially amorphous.

43. A memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a cobalt-titanium alloy oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the cobalt-titanium alloy oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

44. The memory array of claim 43, wherein the cobalt-titanium alloy oxide dielectric layer includes $CoTiO_3$.

45. The memory array of claim 43, wherein the cobalt-titanium alloy oxide dielectric layer exhibits a dielectric constant (k) of approximately 40.

46. The memory array of claim 43, wherein the cobalt-titanium alloy oxide dielectric layer is substantially amorphous.

47. An information handling device, comprising:

a processor;

a memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a cobalt-titanium alloy oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the cobalt-titanium alloy oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

a system bus coupling the processor to the memory device.

48. The information handling device of claim 47, wherein the cobalt-titanium alloy oxide dielectric layer includes $CoTiO_3$.

49. The information handling device of claim 47, wherein the cobalt-titanium alloy oxide dielectric layer exhibits a dielectric constant (k) of approximately 40.

50. The information handling device of claim 47, wherein the cobalt-titanium alloy oxide dielectric layer is substantially amorphous.

51. A transistor formed by the process, comprising:

forming a body region coupled between a first source/drain region and a second source/drain region;

evaporation depositing a metal alloy layer on the body region;

oxidizing the metal alloy layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

52. The transistor of claim 51, wherein evaporation depositing the metal alloy layer includes evaporation depositing cobalt and titanium.

53. The transistor of claim 51, wherein evaporation depositing the metal alloy layer includes evaporation depositing by electron beam evaporation.

54. The method of claim 51, wherein oxidizing the metal alloy layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

55. A method of forming a gate oxide on a transistor body region, comprising:

electron beam evaporation depositing a metal alloy layer on the body region; and

oxidizing the metal alloy layer to form a metal oxide layer on the body region.